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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,737	12/31/2003	Richard Lane	MICS:0110 (02-1455)	1834

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EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,737	LANE, RICHARD	
	Examiner	Art Unit	
	Ida M. Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9,11-15,17-21,23 and 25-29* is/are rejected.

7)☒ Claim(s) *3,7, 10,14, 16,22,24 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed December 31, 2003.

Claim Objections

Claims 7 and 14 are objected to because of the following informalities: "**out**" should have been **outer** on pages 17-18, lines 5 and 11, respectively. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Seshadri et al. (US 6,730,950 B1).

Seshadri et al. teach a memory device 70 comprising: a capacitor C2 having an upper cell plate 76 and a lower cell plate 77; an access transistor 96 coupled directly to the lower cell plate 77 of the capacitor C2 through a first conductive plug 71a; and a transistor 94, wherein the gate 79c of the transistor 94 is coupled directly to the lower

cell plate 77 of the capacitor C2 through a second conductive plug 71c (Figures 6A-6B, columns 9-10, lines 41-53 and 27-65, respectively).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seshadri et al. (US 6,730,950 B1) as applied to claim 1 above, and further in view of Shimada et al. (US 2002/0024073 A1).

Seshadri et al. teach all mentioned in the rejection above. However, Seshadri et al. fail to teach a first conductive plug comprising polysilicon plug, and a second conductive plug comprising a tungsten (metal) plug.

Shimada et al. teach a first conductive plug 21 comprising polysilicon plug; and a second conductive plug 32 comprising a tungsten (metal) plug (Figure 1D, pages 2-3, paragraphs [0027]-[0030]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the memory device structure as taught by Seshadri et al. with the memory device having a first conductive plug comprising polysilicon plug, and a second conductive plug comprising a tungsten (metal) plug as

taught by Shimada et al. to provide a contact member to connect the elements of a memory device (page 2, paragraph [0027]).

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Seshadri et al. (US 6,730,950 B1) as applied to claim 1 above, and further in view of Imai (US 2002/0089059 A1).

Seshadri et al. teach all mentioned in the rejection above. However, Seshadri et al. fail to teach the closest outer edge of the first conductive plug separated from the closest outer edge of the second conductive plug by a distance in the range of approximately 20nm to 50nm.

Imai teaches the closest outer edge of the first conductive plug 9 separated from the closest outer edge of the second conductive plug 9 by a distance in the range 300nm or less (Figure 1E, page 4, paragraphs [0048] and [0051]), which the claimed range of approximately 20nm to 50nm lies within.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device structure as taught by Seshadri et al. with the semiconductor device having the closest outer edge of the first conductive plug separated from the closest outer edge of the second conductive plug by a distance in the range 300nm or less as taught by Imai to prevent the short circuiting of conductive plugs (page 4, paragraph [0051]).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Seshadri et al. (US 6,730,950 B1) in view of DeBoer et al. (US 6,864,527 B2).

In regard to claim 8, Seshadri et al. teach a memory device 70 comprising: a capacitor C2 having an upper cell plate 76 and a lower cell plate 77; an access transistor 96 coupled directly to the lower cell plate 77 of the capacitor C2 through a first conductive plug 71a; and a transistor 94, wherein the gate 79c of the transistor 94 is coupled directly to the lower cell plate 77 of the capacitor C2 through a second conductive plug 71c (Figures 6A-6B, columns 9-10, lines 41-53 and 27-65, respectively).

However, Seshadri et al. fail to teach a system comprising: a processor; and a memory device coupled to the processor.

DeBoer et al. teach a system comprising: a processor; and a memory device coupled to the processor (Figures 1A and 4-5, columns 3 and 8, lines 12-14 and 1-8, respectively).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the memory device structure as taught by Seshadri et al. with the memory device having a system comprising: a processor; and a memory device coupled to the processor as taught by DeBoer et al. to provide a memory device with increased performance (column 1, lines 18-35).

Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seshadri et al. (US 6,730,950 B1) and DeBoer et al. (US 6,864,527 B2) as applied to claim 8 above, and further in view of Shimada et al. (US 2002/0024073 A1).

Seshadri et al. and DeBoer et al. teach all mentioned in the rejection above. However, Seshadri et al. and DeBoer et al. fail to teach a first conductive plug comprising polysilicon plug, and a second conductive plug comprising a tungsten (metal) plug.

Shimada et al. teach a first conductive plug 21 comprising polysilicon plug; and a second conductive plug 32 comprising a tungsten (metal) plug (Figure 1D, pages 2-3, paragraphs [0027]-[0030]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the memory device structure as taught by Seshadri et al. and a memory device coupled to the processor as taught by DeBoer et al. with the memory device having a first conductive plug comprising polysilicon plug, and a second conductive plug comprising a tungsten (metal) plug as taught by Shimada et al. to provide a contact member to connect the elements of a memory device (page 2, paragraph [0027]).

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Seshadri et al. (US 6,730,950 B1) and DeBoer et al. (US 6,864,527 B2) as applied to claim 8 above, and further in view of Imai (US 2002/0089059 A1).

Seshadri et al. and DeBoer et al. teach all mentioned in the rejection above. However, Seshadri et al. and DeBoer et al. fail to teach the closest outer edge of the first conductive plug separated from the closest outer edge of the second conductive plug by a distance in the range of approximately 20nm to 50nm.

Imai teaches the closest outer edge of the first conductive plug 9 separated from the closest outer edge of the second conductive plug 9 by a distance in the range 300nm or less (Figure 1E, page 4, paragraphs [0048] and [0051]), which the claimed range of approximately 20nm to 50nm lies within.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device structure as taught by Seshadri et al. and the semiconductor device coupled to the processor as taught by DeBoer et al. with the semiconductor device having the closest outer edge of the first conductive plug separated from the closest outer edge of the second conductive plug by a distance in the range 300nm or less as taught by Imai to prevent the short circuiting of conductive plugs (page 4, paragraph [0051]).

Claims 2, 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seshadri et al. (US 6,730,950 B1) in view of Takeda et al. (US 2001/0045589 A1).

In regard to claim 15, Seshadri et al. teach a memory device 70 comprising: a first transistor 94 coupled to a second transistor 92; and a memory portion comprising an access transistor 96 and a storage capacitor C2, wherein the storage capacitor comprises a first cell plate 77 configured to form an access node 71 of the memory

device, wherein the source of the access transistor 96 and the gate of the first transistor are coupled to the first cell plate 77 of the storage capacitor (Figures 6A-6B, columns 9-10, lines 41-53 and 27-65, respectively).

In regard to claim 17, Seshadri et al. teach the source of the access transistor 96 coupled to the first cell plate 77 by a first conductive post 71a, and wherein the gate 79c of the first transistor 94 is coupled to the first cell plate 77 by a second conductive post 71c (Figures 6A-6B, columns 9-10, lines 41-53 and 27-65, respectively).

However, Seshadri et al. fail to teach a content addressable memory portion.

In regard to claims 2 and 15, Takeda et al. teach a content addressable memory portion (Figure 3, pages 1 and 3-4, paragraphs [0014] and [0063]-[0072], respectively).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the memory device structure as taught by Seshadri et al. with the memory device having a content addressable memory portion as taught by Takeda et al. to provide a semiconductor device capable of realizing a high performance content addressable memory (page 1, paragraph [0008]).

Claims 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seshadri et al. (US 6,730,950 B1) and Takeda et al. (US 2001/0045589 A1) as applied to claims 2, 15 and 17 above, and further in view of Shimada et al. (US 2002/0024073 A1).

Seshadri et al. and Takeda et al. teach all mentioned in the rejection above. However, Seshadri et al. and Takeda et al. fail to teach a first conductive post and a

second conductive post comprising different types of material, wherein the first conductive post comprises polysilicon, and the second conductive post comprises tungsten (metal).

Shimada et al. teach a first conductive post and a second conductive post comprising different types of material, wherein the first conductive post 21 comprises polysilicon, and the second conductive post 32 comprises tungsten (metal) (Figure 1D, pages 2-3, paragraphs [0027]-[0030]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the memory device structure as taught by Seshadri et al. and the memory device having a content addressable memory portion as taught by Takeda et al. with the memory device having a first conductive post and a second conductive post comprising different types of material, wherein the first conductive post comprises polysilicon, and the second conductive post comprises tungsten (metal) as taught by Shimada et al. to provide a contact member to connect the elements of a memory device (page 2, paragraph [0027]).

Claims 9, 23 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seshadri et al. (US 6,730,950 B1) in view of DeBoer et al. (US 6,864,527 B2) and Takeda et al. (US 2001/0045589 A1).

In regard to claim 23, Seshadri et al. teach a memory device 70 comprising: a first transistor 94 coupled to a second transistor 92; and a memory portion comprising an access transistor 96 and a storage capacitor C2, wherein the storage capacitor

comprises a first cell plate 77 configured to form an access node 71 of the memory device, wherein the source of the access transistor 96 and the gate of the first transistor 94 are coupled to the first cell plate 77 of the storage capacitor (Figures 6A-6B, columns 9-10, lines 41-53 and 27-65, respectively).

In regard to claim 25, Seshadri et al. teach the source of the access transistor 96 coupled to the first cell plate 77 by a first conductive post 71a, and wherein the gate 79c of the first transistor 94 is coupled to the first cell plate 77 by a second conductive post 71c (Figures 6A-6B, columns 9-10, lines 41-53 and 27-65, respectively).

However, Seshadri et al. fail to teach a system comprising: a processor; and a memory device couple to the processor and comprising: a content addressable memory portion.

In regard to claims 23 and 25, DeBoer et al. teach a system comprising: a processor; and a memory device coupled to the processor (Figures 1A and 4-5, columns 3 and 8, lines 12-14 and 1-8, respectively).

And in regard to claims 9 and 23, Takeda et al. teach a content addressable memory portion (Figure 3, pages 1 and 3-4, paragraphs [0014] and [0063]-[0072], respectively).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the memory device structure as taught by Seshadri et al. with the memory device having a system comprising: a processor; and a memory device coupled to the processor as taught by DeBoer et al. and the memory device having a content addressable memory portion as taught by Takeda et al. to

provide a semiconductor device capable of realizing a high speed information processing system (page 1, paragraph [0005]).

Claims 26-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seshadri et al. (US 6,730,950 B1), DeBoer et al. (US 6,864,527 B2) and Takeda et al. (US 2001/0045589 A1) as applied to claims 9, 23 and 25 above, and further in view of Shimada et al. (US 2002/0024073 A1).

Seshadri et al., DeBoer et al. and Takeda et al. teach all mentioned in the rejection above. However, Seshadri et al., DeBoer et al. and Takeda et al. fail to teach a first conductive post and a second conductive post comprising different types of material, wherein the first conductive post comprises polysilicon, and the second conductive post comprises tungsten (metal).

Shimada et al. teach a first conductive post and a second conductive post comprising different types of material, wherein the first conductive post 21 comprises polysilicon, and the second conductive post 32 comprises tungsten (metal) (Figure 1D, pages 2-3, paragraphs [0027]-[0030]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the memory device structure as taught by Seshadri et al., the memory device having a system comprising: a processor; and a memory device coupled to the processor as taught by DeBoer et al. and the memory device having a content addressable memory portion as taught by Takeda et al. with the memory device having a first conductive post and a second conductive post comprising

different types of material, wherein the first conductive post comprises polysilicon, and the second conductive post comprises tungsten (metal) as taught by Shimada et al. to provide a contact member to connect the elements of a memory device (page 2, paragraph [0027]).

Allowable Subject Matter

Claims 3, 10, 16, 22, 24 and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record does not disclose, make obvious, or otherwise suggest the structure of the applicant's together with the other limitations of the independent claims. The closest prior art of record being Aono (4,903,110) teaching a surface area of an capacitor plate (column 1, lines 29-45) and Imai (US 2002/0089059 A1) teaching conductive plugs (Figure 1E, page 4, paragraphs [0048] and [0051]).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to memory devices having capacitors and transistors:

Amo et al. (US 2004/0129963 A1) Fukuda et al. (US 2001/0022369 A1)

Katori et al. (6,011,284) Ma et al. (US 2002/0135005 A1

Nakashima et al. (US 2004/0150019 A1) Tottori (US 6,207,987 B1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
March 18, 2005

Ida M. Soward
AU 2822